

REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed May 4, 2005. The Examiner is thanked for the thorough examination of this application.

Claims 1, 4, 8, 10, 12, 21, 23, 30 and 32 have been amended. Claims 3, 11, 22, 23, and 31 have been cancelled. After entry of the foregoing amendments, claims 2, 5-7, 9, 13-20, 24-29, and 33-41 remain pending in this application. Moreover, Applicants have amended FIGs. 1 and 3 to add reference numerals 20 and 40. In view of the amended drawings, the objections to the drawings, and to the specification, are properly addressed and overcome.

Support for amended claims 1, 10, 21 and 30 can be found at least on page 8 of the application. Specifically, the limitation “nitrogen atoms incorporated along the conductive gate layer sidewall and the gate insulator layer-substrate interface” can be found on page 8, lines 5-9, and FIG. 9. Accordingly, Applicant submits that no new matter has been added to the application by this amendment.

Rejections Under 35 U.S.C. 112 of Claim 8

Claim 8 is amended in accordance with the Examiner’s suggestion. Accordingly, the Applicant requests that the objections to claim 8 be withdrawn.

Rejections Under 35 U.S.C. 102(b) of Claims 1, 3-7, 9, and 21-28

Claims 1, 3-7, 9, and 21-28 were rejected under 35 U.S.C. 102(b) as allegedly unpatentable over Kurooka et al (USPN 6184088, hereinafter “Kurooka”). Claims 1 and 21 are independent claims, from which claims 2-9 and 22-28 depend. Applicant asserts that claims 1 and 21 are patentable for the reasons discussed below, and therefore for at least the same reasons claims 2-9 and 22-28 are patentable.

The Office Action alleges that “Kurooka discloses a split gate transistor that contains a semiconductor region, at least a gate stack containing a gate insulator layer and a conductive gate layer disposed over said gate insulator layer with nitrogen atoms 70a incorporated along the conductive gate layer sidewall.”

Amended claim 1 recites:

1. A gate structure, comprising:
 - a semiconductor region within a substrate;
 - source and drain regions contained within said semiconductor region; at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive gate layer disposed over said gate insulator layer, *with nitrogen atoms incorporated along the conductive gate layer sidewall and the gate insulator layer-substrate interface.*

Amended claim 21 recites:

21. A method to fabricate a gate structure, comprising:
 - providing a semiconductor region within a substrate;
 - forming source and drain regions contained within said semiconductor region;
 - forming at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive gate layer disposed over said gate insulator layer and *providing a nitrogen-based treatment on the sidewall of said conductive gate layer and the gate insulator layer-substrate interface.*

(Emphasis Added)

It is clear that the claimed gate structure includes a conductive gate layer **with nitrogen atoms incorporated along the conductive gate layer sidewall and the gate insulator layer-substrate interface**, as recited in claim 1. Likewise, claim 21 also defines that the method to fabricate a gate structure comprises **providing a nitrogen-based treatment on the sidewall of said conductive gate layer and the gate insulator layer-substrate interface**. Thus, it can be seen that the nitrogen atoms in claims 1 and 21 are not merely incorporated along the conductive gate layer sidewall, but also into the gate insulator layer-substrate interface.

In contrast, as disclosed by Kurooka in column 10, lines 44-49 and FIG 12C:

“The nitrogen-containing layer 70a maybe formed according to the following methods:
(a) The lateral faces of the floating gate electrode 70 are exposed to nitrogen plasma; or (b)
After formation of the floating gate electrode 70, it is subjected to thermal treatment in an
atmosphere containing nitrogen (NH₃ or the like).”

Referring to Kurooka, the lateral faces of the floating gate electrode 70 are exposed to nitrogen plasma or by thermal treatment in an atmosphere containing nitrogen after formation of the floating gate electrode 70. However, Kurooka does not disclose **nitrogen atoms further extending to the interface of the gate insulator layer-substrate in the vicinity of the conductive gate layer edge**, as recited in claim 9 (Applicants understand that the feature of claim 9 is not a part of independent claims 1 and 21, but is cited here as relevant to a proper interpretation of claims 1 and 21, pursuant to the Doctrine of Claim Differentiation). Accordingly, the conductive gate layer sidewall incorporated with nitrogen atoms in claims 1 and 21 is clearly and structurally different from the nitrogen-containing layer 70a in “Kurooka” since the nitrogen-containing layer 70a cannot provide the nitrogen atoms in vicinities of the conductive gate layer sidewall, and the interface and edge of the conductive gate layer-gate insulator layer and the gate insulator layer-substrate. For at least these reasons, reconsideration of this rejection is hereby respectfully requested.

Hence it is respectfully asserted that amended claims 1 and 21 are allowable over the cited reference (Kurooka et al). Insofar as claims 2-9 and 22-28 depend from amended claims 1 and 21, it is Applicant’s assertion that these claims are also allowable at least by virtue of their dependency from allowable claims.

Rejections Under 35 U.S.C. 103(a) of Claims 2 and 8

Insofar as claims 2 and 8 separately depend from amended claim 1, these claims are also allowable at least by virtue of their dependency from an allowable claim.

Reconsideration of the above rejection of claims 2 and 8 is hereby respectfully requested.

Rejections Under 35 U.S.C. 103(a) of Claims 10-20, 30-37, and 39-41

Claims 10-20, 30-37, and 39-41 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Kurooka et al. in view of Applicant's Prior Art. Claims 10 and 30 are independent claims, from which claims 11-20 and 31-41 depend. Applicants submit that claims 10 and 30 is patentable for the reasons discussed below, and therefore for at least the same reasons claims 11-20 and 31-41 are patentable.

The Office Action asserts that "Kurooka discloses a conductive gate layer *with nitrogen atoms 70a incorporated along the conductive gate layer sidewall*. In addition, one having ordinary skill in the art can modify the device of Applicant's Prior Art by incorporating nitrogen atoms on the sidewall of the floating gate to minimize the dangling bond of the native oxide film and to prevent bird's beak from being formed on the tunnel insulating layer as taught by Kurooka."

Amended claim 10 recites:

10. A gate structure for flash memory cells, comprising:
 - a semiconductor region within a substrate;
 - source and drain regions contained within said semiconductor region;
 - at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive floating gate layer over said gate insulator layer, an interpoly insulator layer disposed over said conductive gate layer, a conductive control gate layer and a top insulator layer and with a sidewall insulator layer disposed over sidewalls of said gate stack and with nitrogen atoms incorporated along the conductive gate layer sidewall-sidewall insulator layer interface and along the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge *and the gate insulator layer-substrate interface*.

Amended claim 30 recites:

30. A method to fabricate a gate structure for flash memory cells, comprising:
 - forming a semiconductor region within a substrate;
 - forming source and drain regions contained within said semiconductor region;
 - forming at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive floating gate layer disposed over said gate insulator layer, an interpoly insulator layer disposed over said conductive gate layer, a conductive control gate layer and a top insulator layer and with a sidewall insulator layer disposed over sidewalls of said gate stack and with a nitrogen treatment performed

which further incorporated into the gate insulator layer-substrate interface before forming said sidewall insulator.

(Emphasis Added)

It is clear that the claimed gate structure for flash memory cells includes a conductive control gate layer with **nitrogen atoms incorporated along the conductive gate layer sidewall-sidewall insulator layer interface and along the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge and the gate insulator layer-substrate interface**, as recited in claim 10.

Besides, claim 30 also states that the method to fabricate a gate structure for flash memory cells comprises forming a conductive control gate layer **with a nitrogen treatment performed which further incorporated into the gate insulator layer-substrate interface**. Thus, it can be seen that the nitrogen atoms in claims 10 and 30 are not merely incorporated along the conductive gate layer sidewall and further incorporated into the gate insulator layer-substrate interface. Moreover, referring to the specification, nitrogen atoms are utilized for the reduction of the electron trap concentration thereof (to fulfill bonds thereof).

However, as disclosed by Kurooka in column 9, lines 3-10:

“While the process proceeds from step 4 to step 5, the lateral faces of the floating gate electrode 70 may be exposed to the outside air containing oxygen. However, *since the nitrogen-containing layer 70a is formed on them*, it is possible to control the formation of a native oxide film, which contains dangling bonds and does not have the O-Si-O bond on the surface of lateral faces of the floating gate electrode 70.”

(Emphasis Added)

Referring to Kurooka, this reference is also silent about **nitrogen atoms further extend to the interface of the gate insulator layer-substrate in the vicinity of the conductive gate layer edge**, as recited in claims 10 and 30. Moreover, he does not disclose nitrogen atoms incorporated along the conductive gate layer sidewall for the reduction of the electron trap concentration thereof (to fulfill bonds thereof). Accordingly, the conductive gate layer sidewall incorporated with nitrogen atoms is apparently

different from the nitrogen-containing layer 70a in "Kurooka". Besides, the nitrogen-containing layer 70a cannot provide the reduction of the electron trap concentration (fulfill bonds) in vicinities of the conductive gate layer sidewall. Reconsideration of this rejection is hereby respectfully requested.

Hence it is respectfully asserted that amended claims 10 and 30 are allowable over both cited references. Insofar as claims 11-20 and 31-41 depend from amended claims 10 and 30, these claims are also allowable at least by virtue of their dependency on allowable claims. Furthermore, insofar as claims 29 and 38 separately depend from amended claim 20 and 30, these claims are also allowable over Kurooka in view of Aminzadeh (USPN 5827769) at least by virtue of their dependency on allowable claims.

Cited Art of Record


The cited art of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this Amendment and Response. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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In the Drawings

In FIG. 1, reference numeral 20 is added to designate the two arrow pointing down and to the left, as shown in the accompanying annotated sheet.

In FIG. 3, reference numeral 40 is added, as shown in the accompanying annotated sheet.

Attachments

Annotated sheets for FIGS 1&2, and 3&4.

Replacement sheets for FIGS 1&2, and 3&4.



Annotated Sheet

1/5

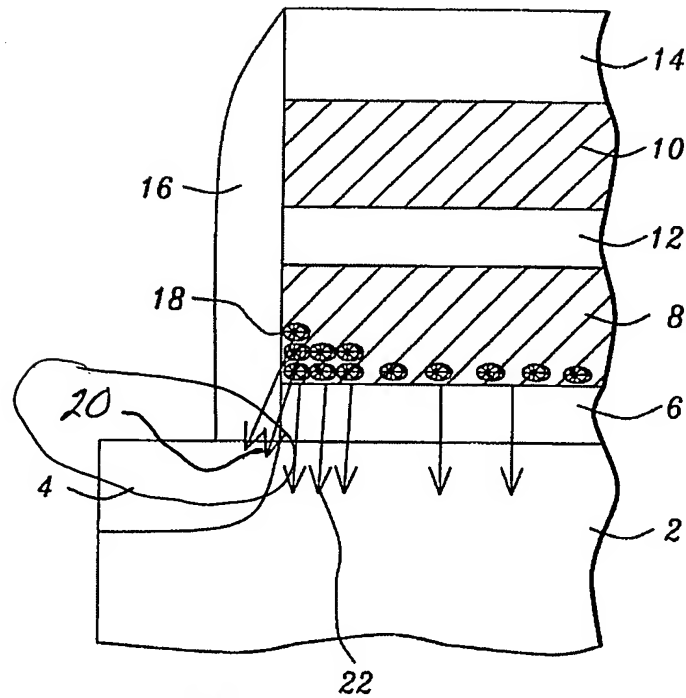


FIG. 1 - Prior Art

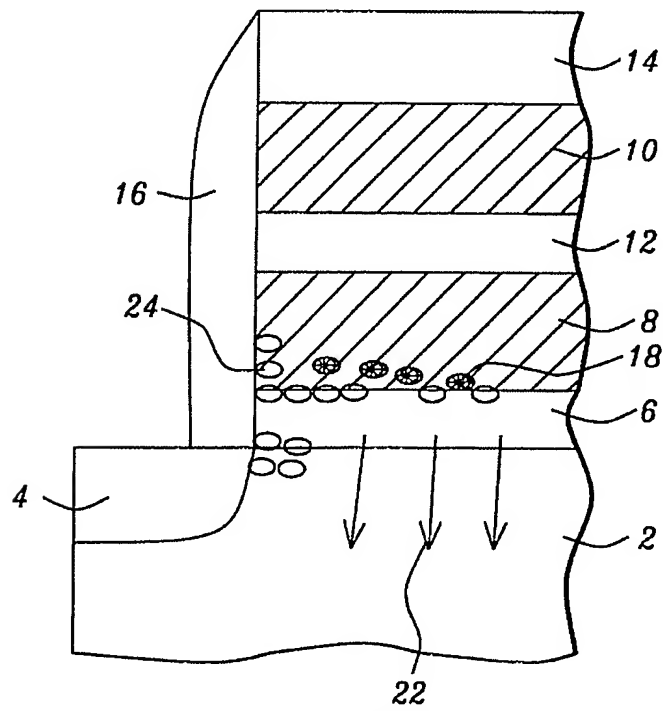


FIG. 2 - Prior Art

Annotated Sheet

2/5

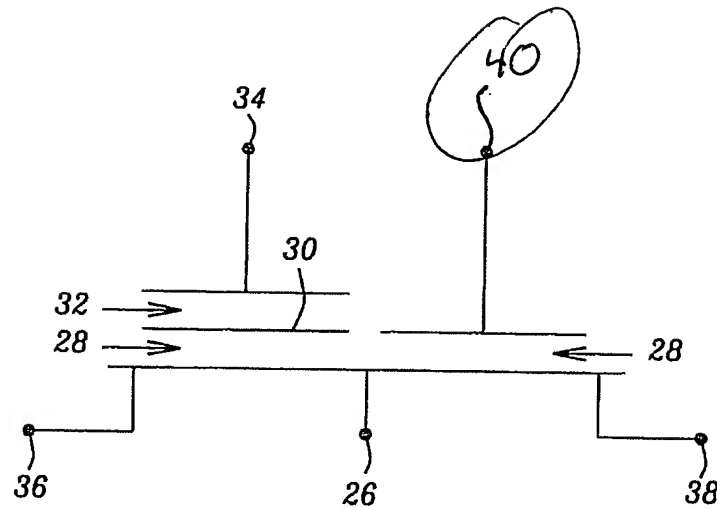


FIG. 3

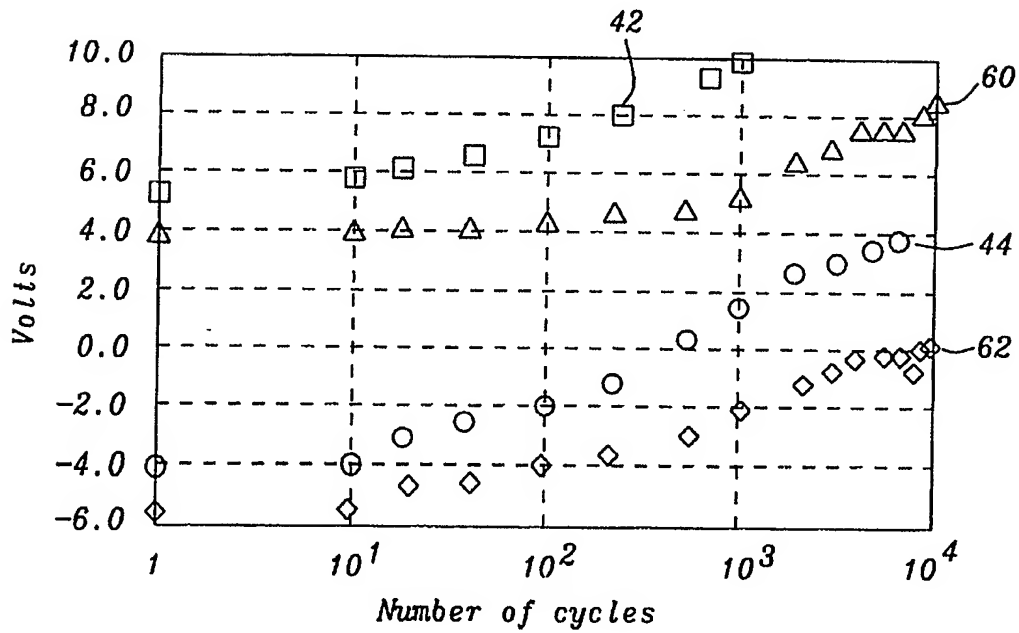


FIG. 4